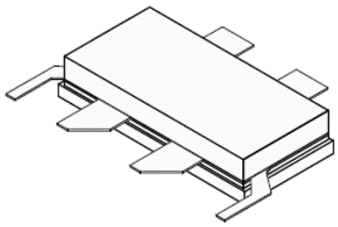
RoHS

LDMOS RF Power Transistor

HTN7G21P160H

1. Features

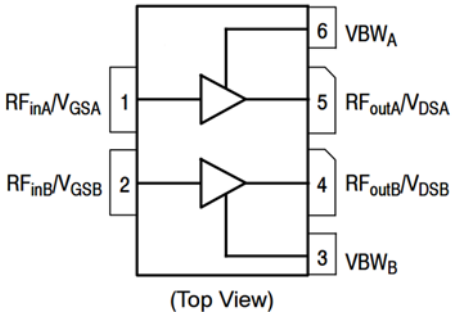
- Advanced High Performance In-Package Doherty
- Grater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction System
- Designed for Wide Instantaneous Bandwidth Applications
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Excellent Robustness
- Excellent Thermal Stability
- RoHS Compliant



Package：H2110S-6L

2. Applications

- GSM EDGE
- MC-GSM
- CDMA
- W-CDMA
- LTE
- WiMAX



Pin Connections

3. Items for Ordering

Type	Package Description	Package Name
HTN7G21P160H	Earless flanged ceramic package; 6 leads	H2110S-6L

4. Typical Performances

This RF LDMOS transistor is designed for base station applications covering the frequency range of 1800MHz to 2200MHz.

Table 1. Single-Carrier WCDMA typical performances

VDD=28V, IDQA=600mA, VGSB=0.7V, Pout=44.8dBm（30W）Avg. Input signal PAR=9.9dB @0.01% Probability on CCDF, in Huatai Test Fixture.

Frequency (MHz)	Gain (dB)	Efficiency (%)	Output PAR (dB)	ACPR (dBc)
1880	16.3	39.2	7.8	-32
1960	16.7	39.6	7.8	-35
2025	16.5	39.4	7.6	-37

5. Maximum Ratings

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Drain to Source Voltage	V_{DSS}	-0.5, +65	V
Gate to Source Voltage	V_{GS}	-5.0, +10	V
Storage Temperature Range	T_{stg}	-55 to +150	℃
Operating Junction Temperature Range	T_J	-40 to +225	℃

6. Thermal Characteristics

Table 3. Thermal Characteristics

Parameter	Symbol	Conditions	Value	Unit
Thermal Resistance (Junction to Packing flange)	$R_{\theta JC}$	Case Temperature：80℃ CW Output Power：160W	0.4	℃/W

7. Electrical Characteristics

Table 4.Electrical Characteristics

Parameter	Symbol	Conditions	Min	Type	Max	Unit
Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V; I_D=108uA	65	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}; I_D=108uA	-	1.5	-	V
Drain Leakage Current	I_{DSS}	V_{DS}=65V; V_{GS}=0V	-	-	10	uA
Gate Leakage Current	I_{GSS}	V_{DS}=0V; V_{GS}=10V	-	-	1	uA
Drain to Source on-State Resistance	$R_{DS(on)}$	V_{GS}=10V; I_D=540mA	-	100	-	mΩ

Table 5. ESD Characteristics

Conditions	Grade
HBM(JESD22--A114)	1B
MM (EIA/JESD22--A115)	A
CDM(JESD22--C101)	III

Table 6. Load Mismatch（*in Huatai Test Fixture*）

Conditions	Results
VSWR=10:1 at all Phase Angles CW: VDD=28V, f=1960MHz, IDQA=600mA, VGGB=0.7V, Pout=160W	No Device Degradation

Table 7. Typical Performances（*in Huatai Test Fixture*）

Characteristic	Symbol	Min	Type	Max	Unit
VDD=28V, IDQA=600mA, VGGB=0.7V, Pout=44.8dBm (30W), Avg. f=1960MHz, Single-Carrier W-CDMA, Input Signal PAR=9.9dB @0.01% Probability on CCDF. ACPR measured in 3.84MHz Channel Bandwidth @ ±5MHz Offset.					
Power Gain	G_{ps}	-	16.6	-	dB
Drain Efficiency	η_D	-	39.6	-	%
Adjacent Channel Power Ratio	ACPR	-	-35.0	-	dBc
Output Signal Peak-to-Average Ratio	PAR	-	7.8	-	dB
VDD=28V, IDQA=600mA, VGGB=0.7V, Pulsed CW					
Pout @ 1dB Compression Point	P1dB	-	51.0	-	dBm
Pout @ 3dB Compression Point	P3dB	-	52.7	-	dBm
AM/PM (Maximum value measured at the P3dB compression point across the 1880-2025MHz frequency range.)	Φ	-	-29	-	°
VBW （IMD third order intermodulation inflection point）	VBW_{res}	-	100	-	MHz
Gain Flatness in 145MHz Bandwidth @ Pout=44.8dBm (30W) Avg.	G_F	-	0.4	-	dB

8. Load-Pull Performance

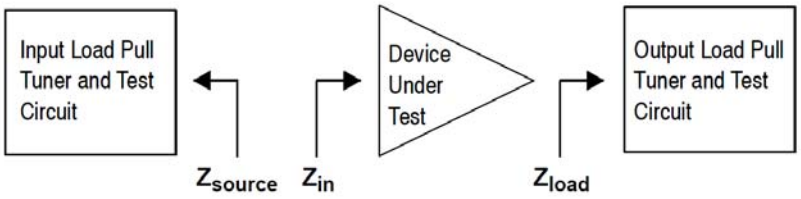
Single Side, V_{DD}=28V, I_{DQ}=300mA, 40us Pulse Width, 4% Duty

Table 8. Load-Pull P3dB — Maximum Power Tuning

f (MHz)	Z_{source} (Ω)	Max Output Power				
		P3dB				
		Z_{load} (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)
1880	2.4-j9.8	1.7-j6.9	18.9	51.3	134.9	58.4
2025	7.5-j13.3	1.7-j7.9	18.9	51.2	131.8	56.4

Table9. Load-Pull P3dB — Maximum Drain Efficiency Tuning

f (MHz)	Z_{source} (Ω)	Max Drain Efficiency				
		P3dB				
		Z_{load} (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)
1880	2.4-j9.8	2.8-j5.1	21.7	49.2	83.2	67.7
2025	7.5-j13.3	2.3-j6.0	21.5	49.3	85.1	65.3



9. Reference Design

9.1 1880MHz-2025MHz Layout of Test Circuit

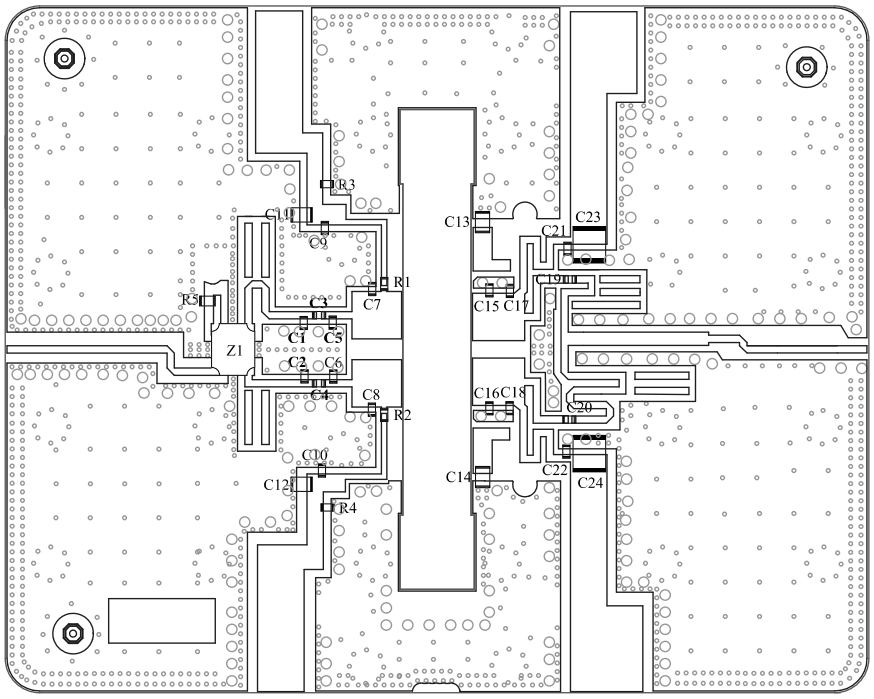


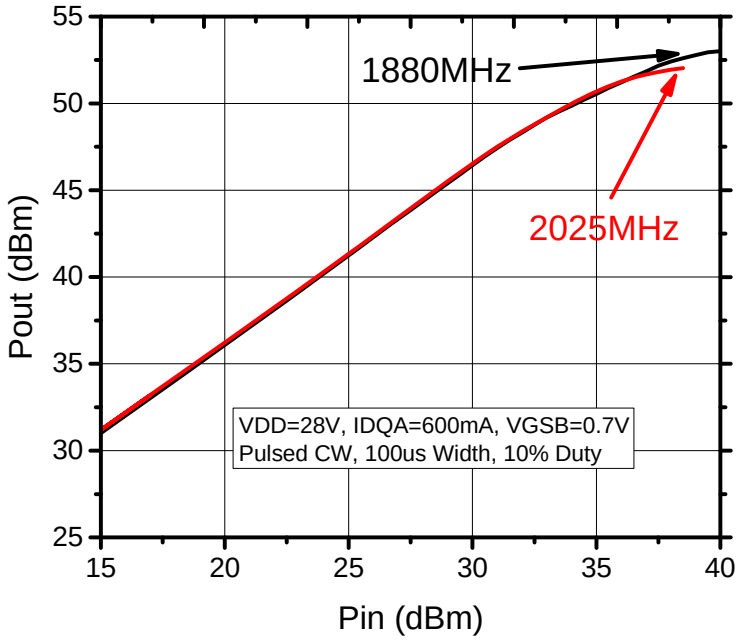
Table 10. 1880MHz-2025MHz Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C3, C4, C9, C10, C19, C20, C21, C22	10pF Chip Capacitors	ATC600S100BT250XT	ATC
C1, C2, C5, C6	0.5pF Chip Capacitors	ATC600S0R8 BT250XT	ATC
C7, C8	1.5pF Chip Capacitors	ATC600S1R5 BT250XT	ATC
C15, C16	2.7pF Chip Capacitors	ATC600S2R7 BT250XT	ATC
C17, C18	0.8pF Chip Capacitors	ATC600S0R8 BT250XT	ATC
C11, C12	10uF Chip Capacitors	Arbitrary	Arbitrary
C13, C14	4.7uF Chip Capacitors	C3225X7S2A475M200AB	Murata
C27, C28	10uF Chip Capacitors	22201C106MAT2A	AVX
R1, R2	10ohm, 1/4W Chip Resistors	Arbitrary	Arbitrary
R3, R4	10Kohm, 1/4W Chip Resistors	Arbitrary	Arbitrary
R5	50ohm, 10W Chip Resistors	Arbitrary	Arbitrary
Z1	1700-2000MHz Band, 90º, 3dB Hybrid	1P503S	Anaren
PCB	RO4350B, 20mil, ε_r = 3.66	--	Rogers

Typical Performances — Pulsed Signal

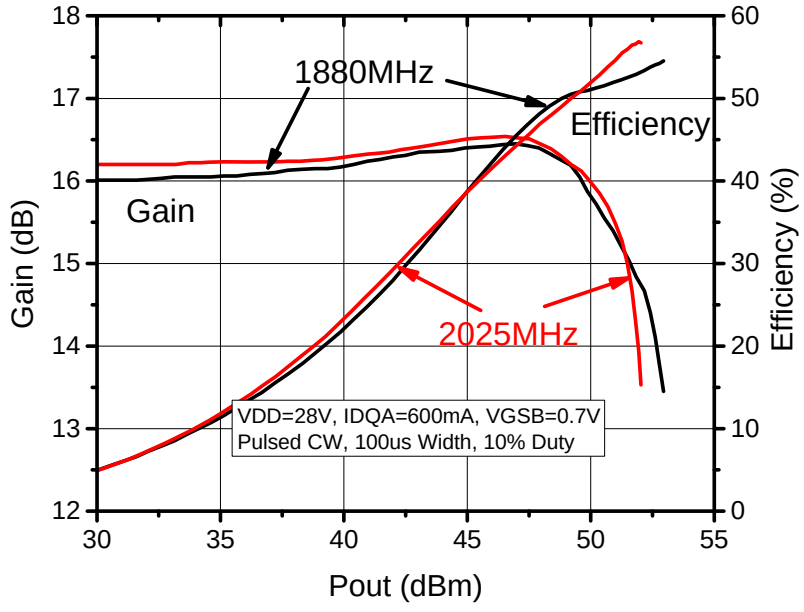
Output Power vs Input Power with Pulsed Signal

VDD=28V, IDQA=600mA, VGSB=0.7V, 100us Pulse Width，10% Duty.



Gain, Efficiency vs Output Power

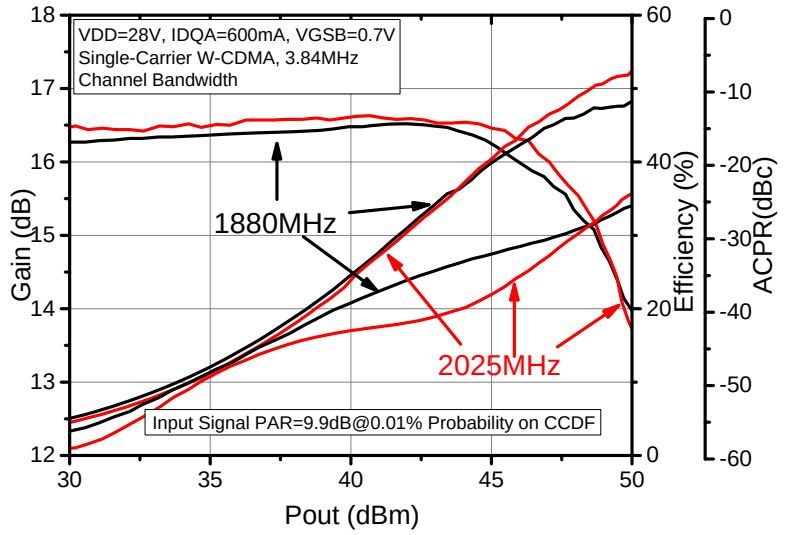
VDD=28V, IDQA=600mA, VGSB=0.7V, 100us Pulse Width，10% Duty.



Typical Performances — Single Carrier W-CDMA

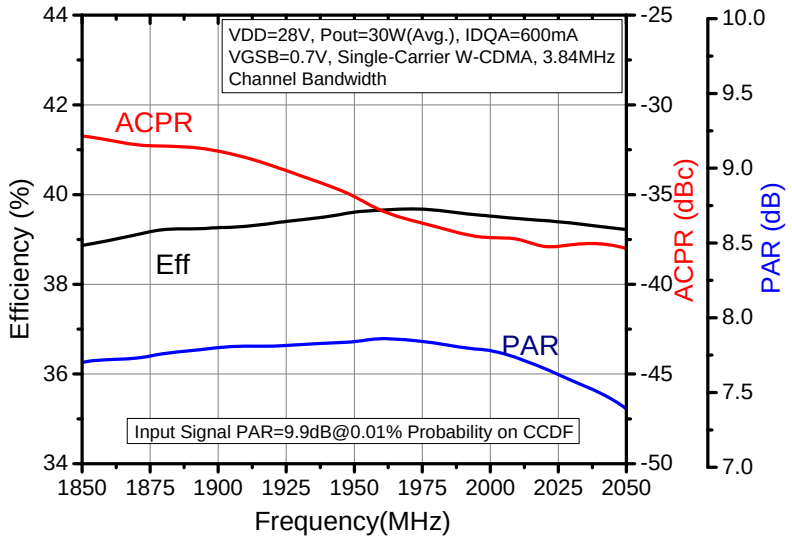
Gain, Efficiency, ACPR vs Output Power

VDD=28V, IDQA=600mA, VGSB=0.7V, Single-Carrier W-CDMA, Input Signal PAR=9.9dB @0.01% Probability on CCDF.



Efficiency, ACPR, PAR vs Frequency @ Pout=30W Avg.

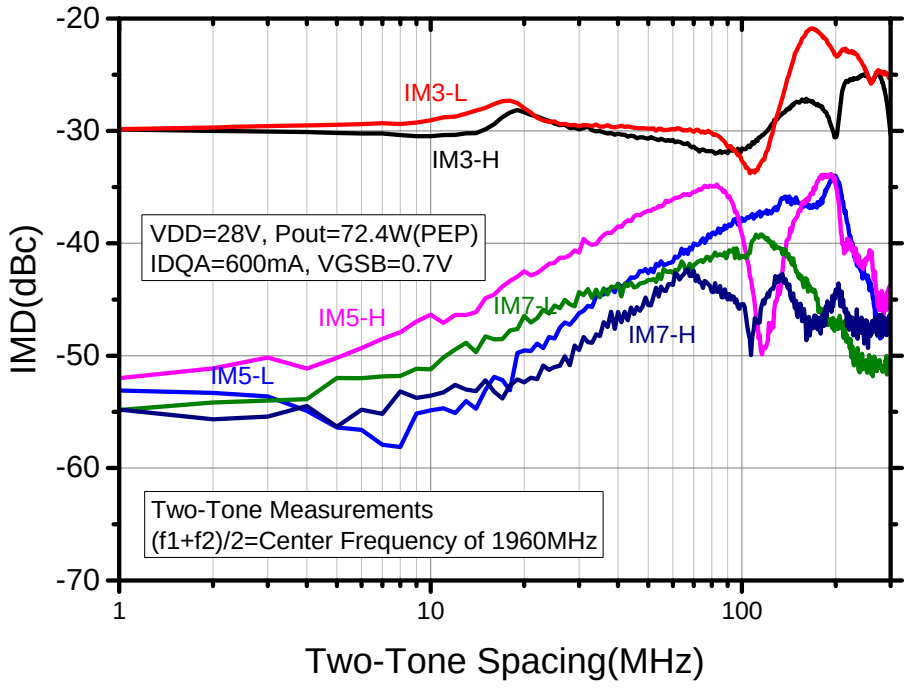
VDD=28V, IDQA=600mA, VGSB=0.7V, Single-Carrier W-CDMA, Input Signal PAR=9.9dB @0.01% Probability on CCDF.



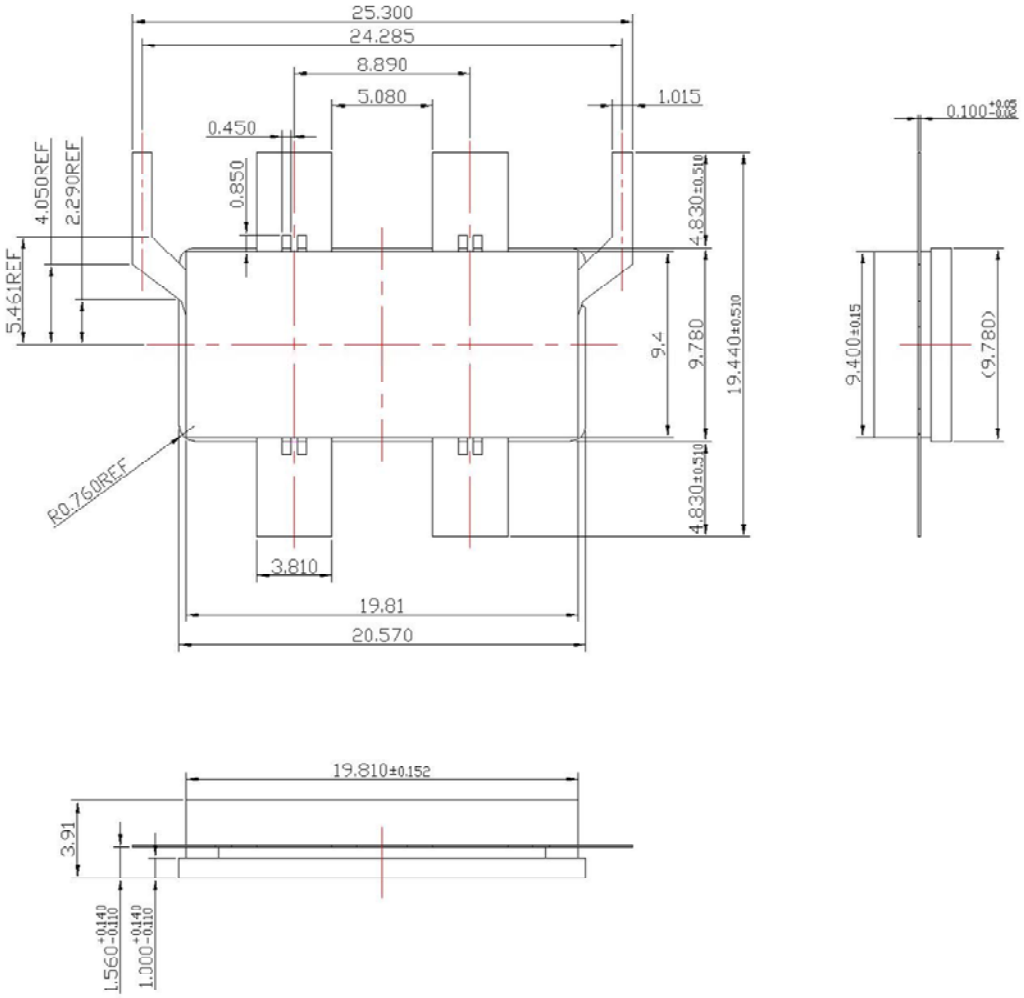
Typical Performances —Intermodulation Distortion Products

Intermodulation Distortion Products vs Two-Tone Spacing @ Pout=72.4W PEP.

VDD=28V，IDQA=600mA，VGSB=0.7V，f=1960MHz



10. Package Dimensions



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