

DATA SHEET

LXK6202: 0.5 - 6.0 GHz SPDT Switch

Applications

■ WiMAX 802.16

■ Dual-band WLANs (802.11 a/b/g/n/ac)

■ LTE/4G systems

Features

Low insertion loss: 0.7dB@2.5GHzHigh isolation: 30dB@2.5GHz

■ IP1dB=+39dBm

■ Small, DFN (6-pin,1.6x1.6 mm) package

Product Description

The LXK6202 is a Single-Pole, Double-Throw (SPDT) high power switch with 50Ω matched outputs. The high linearity performance and low insertion loss achieved by the LXK6202 make it an ideal choice for WiMAX and higher power WLAN applications such as access points.

The switch is manufactured in a compact, 1.6 x 1.6 mm, 6-pin Dual Flat No-Lead (DFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

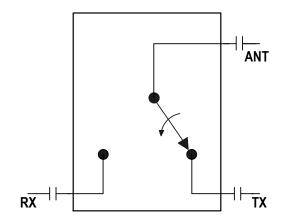


Figure 1. LXK6202 Block Diagram

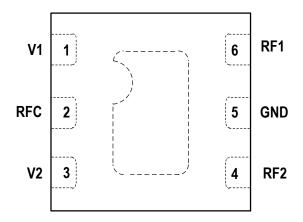


Figure 2. LXK6202 Pinout-6-Pin DFN (Top View)

Table 1. LXK6202 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	V1	DC control voltage. A logic high voltage	4	RF2	RF output 2. Must be DC blocked.
		enables a connection path between the			
		RFC and RF1 pins.			
2	RFC	RF common input. Must be DC	5	GND	Ground
		blocked.			
3	V2	DC control voltage. A logic high voltage	6	RF1	RF output 1. Must be DC blocked.
		enables a connection path between the			
		RFC and RF2 pins.			

Table 2. LXK6202 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Control voltage	VCTL			6	V
Input power	PIN			40	dBm
Storage temperature	TSTG	-40		125	°C
Operating temperature	TOP	-40		85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Functional Description

Switching is controlled by two control voltage inputs, V1 and V2 (pins 1 and 3, respectively). Depending on the logic voltage level applied to the control pins, the RFC pin is connected to one of the two switched RF outputs, RF1 or RF2, using a low insertion loss path, while the path between the RFC pin and the other RF pin is in a high isolation state. DC blocking capacitors are required on all RF ports of the switch. The value of the capacitors determines the low frequency operation.

Electrical and Mechanical Specifications

The absolute maximum ratings of the LXK6202 are provided in Table 2. Electrical specifications are provided in Table 3. Typical performance characteristics of the LXK6202 are illustrated in Figures 3 through 6. The state of the LXK6202 is determined by the logic provided in Table 4.

Table 3.LXK6202 Electrical Specifications

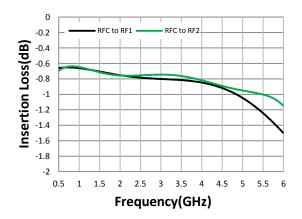
(V_{CTL}=0V and +3.0 V, T_{OP}=+25 °C, PIN=0dBm,Characteristic Impedance [Z_o]= 50 Ω ,CBL=47 pF, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
RF Specifications						
Insertion loss	IL	RFC to RF1 or RF2: 0.50 to 2.70 GHz 2.70 to 3.80 GHz 3.80 to 5.85 GHz		0.7 0.8 1.0	0.8 0.9 1.4	dB dB dB
Isolation	Iso	RFC to RF1 or RF2: 0.50 to 2.40 GHz 2.40 to 2.50 GHz 2.50 to 3.80 GHz 3.80 to 5.85 GHz		31 30 30 30		dB dB dB dB
Input return loss ("on" state)	S11	RFC or RF1 or RF2: 0.50 to 6.0 GHz		16		dB
1 dB Input Compression Point	IP1dB	VCTL = 3.0 V: 1.80 to 2.00 GHz 2.30 to 2.70 GHz 3.30 to 3.80 GHz 4.90 to 5.85 GHz		39 39 39 39		dBm dBm dBm dBm
3rd Order Input Intercept Point	IIP3	PIN = +25 dBm/tone, △f=1 MHz VCTL=3.0V: 1.8 GHz 2.4 GHz 3.8 GHz 5.8 GHz		55 55 55 55		dB dB dB dB
2nd harmonic	2fo	PIN = +25 dBm, VCTL=3.0V: 0.9GHz 1.8GHz 2.4GHz 3.8GHz 5.8GHz		75 75 75 75 75		dBc dBc dBc dBc dBc
3rd harmonic	3fo	PIN = +25 dBm, VCTL=3.0V: 0.9GHz 1.8GHz 2.4GHz 3.8GHz 5.8GHz		75 75 75 75 75		dBc dBc dBc dBc dBc
Switching speed		50% VCTL to 90/10% RF 90/10% RF or 10/90% RF		100 100		ns ns
DC Specifications		20, 10,001,11 0, 10,007,011	l 	100	l	110
Control voltage Control current	VCTL ICC		2.5	3 5	5	V µA

Note: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(V_{CTL}=0V and +3.0 V, T_{OP}=+25 °C, PIN=0dBm, Characteristic Impedance [Z_o]= 50 Ω, CBL=47 pF, Unless Otherwise Noted)



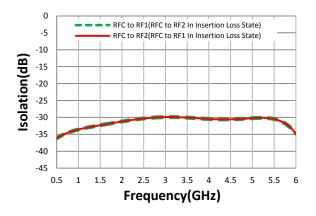
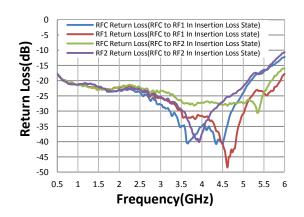


Figure 3. Typical Insertion Loss vs Frequency

Figure 4. Typical Isolation vs Frequency





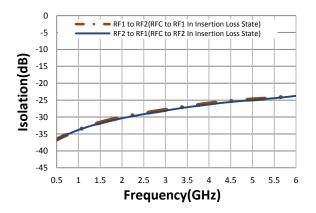


Figure 6.Typical Isolation vs Frequency (RF1 to RF2)

Table 4. LXK6202 Truth Table

V1 (Pin 1)	V2 (Pin 3)	Insertion Loss State
1	0	RFC to RF1
0	1	RFC to RF2

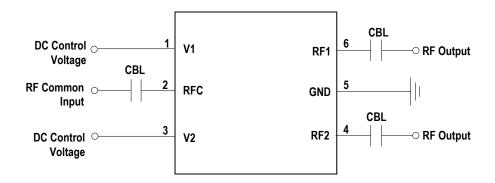
Note: "1" = +2.5V to +5.0V. "0" = 0 V to +0.2 V. Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.

Evaluation Board Description

The LXK6202 Evaluation Board is used to test the performance of the LXK6202 SPDT Switch. An Evaluation Board schematic diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

Package Diagram

The LXK6202 is housed in a 6-pin Dual Flat No-Lead (DFN) package. Package dimensions for the 6-pin DFN are shown in Figure 9.



CBL=47pF for >1GHz operation. Increase value for lower frequency operation.

Figure 7. LXK6202 Evaluation Board schematic

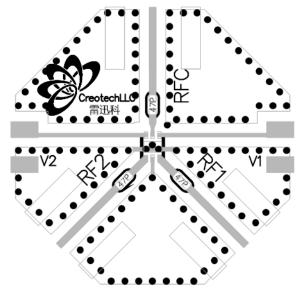
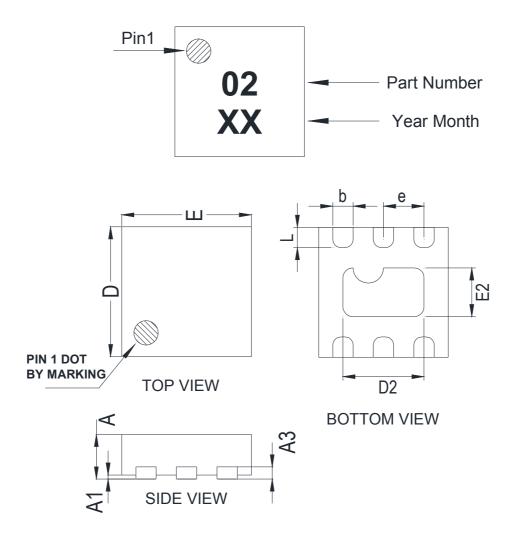


Figure 8. LXK6202 Evaluation Board Assembly Diagram

Package Diagram



COMMON DIMENSIONS (MM)				
REF.	MIN.	NOM.	MAX.	
Α	0.50	0.55	0.60	
A1	0.00	-	0.05	
A3		0.15REF.		
D	1.55	1.60	1.65	
Е	1.55	1.60	1.65	
D2	0.90	1.00	1.05	
E2	0.50	0.60	0.65	
L	0.20	0.25	0.30	
b	0.20	0.25	0.30	
е		0.50 BSC		

Figure 9. LXK6202 6-Pin DFN Package Dimensions

Ordering Information

Part No.	Description
LXK6202	Switch
EVB-LXK6202-01	Evaluation Board

Document Change History

Revision	Date	Notes
1.0	June 19, 2014	Created

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