CREOTECH

DATA SHEET

LXK6618: High Efficiency 1.6 GHz 5 W Power Amplifier

Applications

- Beidou handheld RF module
- GNSS Satellite communication
- GPS systems
- Beidou systems

Features

- Frequency band: 1600 to 1650MHz
- PA output power (P1dB): 37 dBm
- Power added efficiency: 45%
- 50 Ohm input internally matched
- High gain: 29 dB
- Active bias circuit
- Temperature compensation
- QFN (20-pin,5mm x 5mm x0.8mm)

Product Description

The LXK6618 is a high-power, high-gain, high-efficiency power amplifier (PA). The device has been designed for use as the final RF amplifier in high performance Global Navigation Satellite System (GNSS) applications including Beidou global navigation positioning system. The device is internally matched to 50 Ohms at the input and the output can be easily matched to obtain optimum power and efficiency characteristics.

The LXK6618 is housed in a miniature 20-pin, 5mm x 5mm x 0.8mm QFN package. A power detector is also included on-chip. The compact footprint coupled with high gain and high efficiency makes LXK6618 an ideal choice as a power amplifier for GNSS systems.

A functional block diagram of LXK6618 is shown in Figure 1. The 20-pin, 5x5 QFN package and pinout are provided in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

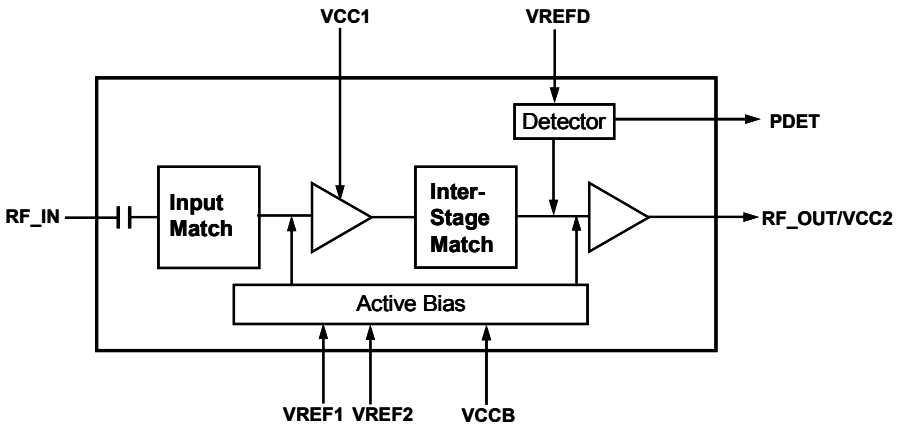


Figure 1. LXK6618 Functional Block Diagram

Table 1. LXK6618 Pin Names and Descriptions

Pin	Name	Description
2	VCCB	Power supply for bias control circuit
3	VCC1	Power supply for stage-1
4	PDET	Detector output voltage for output power
7	RF_IN	RF input
9	VREFD	Reference voltage for detector circuit
10	VREF1	Reference voltage for stage-1 bias
11	VREF2	Reference voltage for stage-2 bias
16, 17, 18, 19, 20	RF_OUT/VCC2	RF output & power supply for stage-2
1, 5, 6, 8, 12, 13, 14, 15	NC	Not connected. May connect to ground.

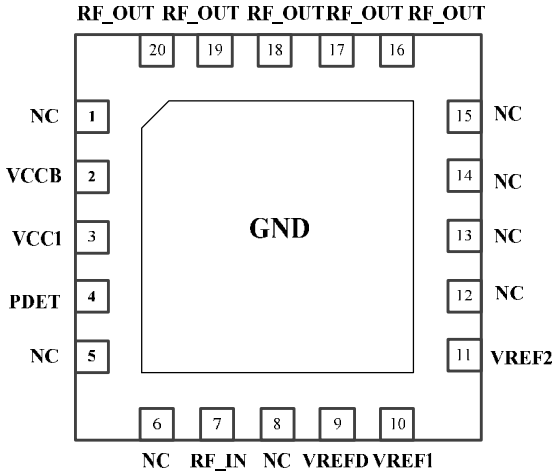


Figure 2. LXK6618 Pinout - 20 pin 5x5 QFN

Table 3. Absolute Maximum Ratings

Parameters	Symbol	Minimum	Maximum	Units
RF input power (CW)	Pin		15	dBm
Supply voltage	V_{CC}		5.5	V
Reference voltages	VREF1,VREF2		3.0	V
Total Supply Current	I_{CC}		3.5	A
Storage temperature	T_{STG}	-40	125	^{O}C
Operating temperature	T_A	-40	75	^{O}C
Junction temperature	T_J		150	^{O}C
Electrostatic Discharge, Human Body Model	ESD		1000	V

Table 4. Recommended Operating Conditions

Parameters	Symbol	Minimum	Typical	Maximum	Units
Operating frequency	f	1600		1650	MHz
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Reference voltages	VREF1, VREF2, VREFD	2.55	2.63	2.7	V
RF output power at P1dB	P1dB		37		dBm
Total supply current at P1dB	I_{CC}		2200		mA
Operating temperature	T_A	-40		75	^{O}C

Table 5. Electrical Specifications

(VCC=5V, VREF1=VREF2=2.6V, Ta=+25 °C, Zs=50Ω, f=1625MHz, CW)					
Parameters	**Test Condition**	**Minimum**	**Typical**	**Maximum**	**Units**
Frequency		1600		1650	MHz
Supply voltage		4.5	5	5.5	V
P1dB			37		dBm
Maximum Output Power			38.2		dBm
Quiescent current			510		mA
VREF1, VREF2			2.63		V
|S11|			-10		dB
|S21|			29		dB
|S12|			-46		dB
PAE	Pout=37dBm		45		%
Output Load VSWR	No damage	10:1			

Typical Performance Characteristics

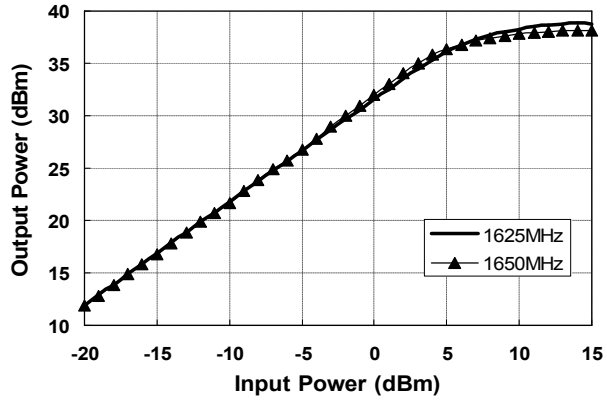


Figure 3. Output power vs input power over frequency at room temperature.

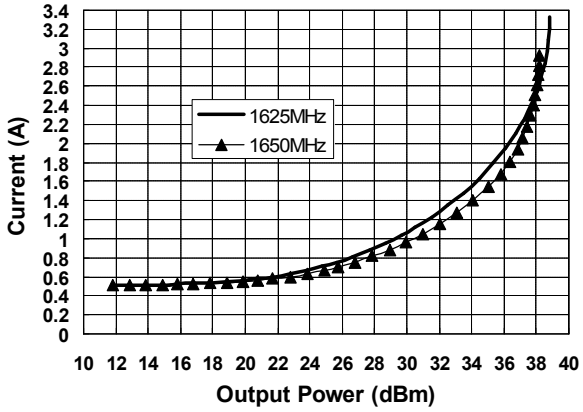


Figure 4. Current vs output Power (CW) over frequency.

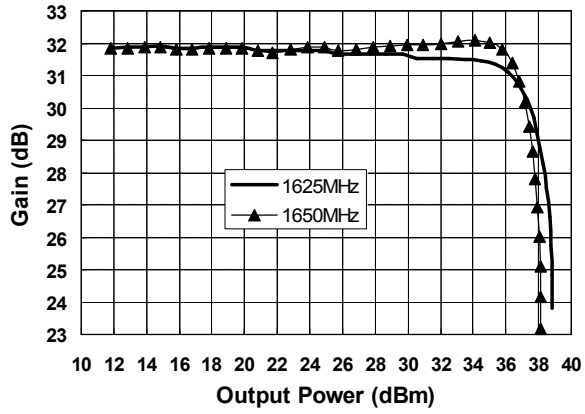


Figure 5. Gain vs output power over frequency.

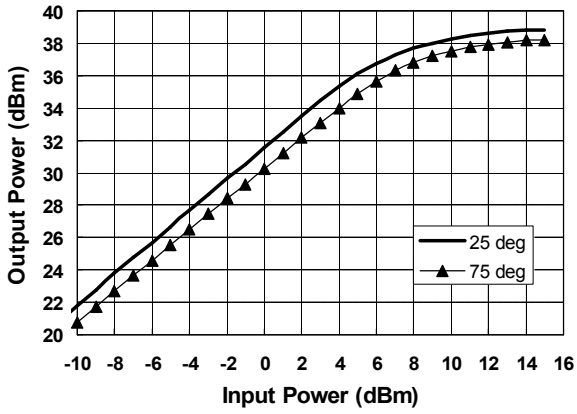


Figure 6. Output power vs input power over temperature at 1625 MHz.

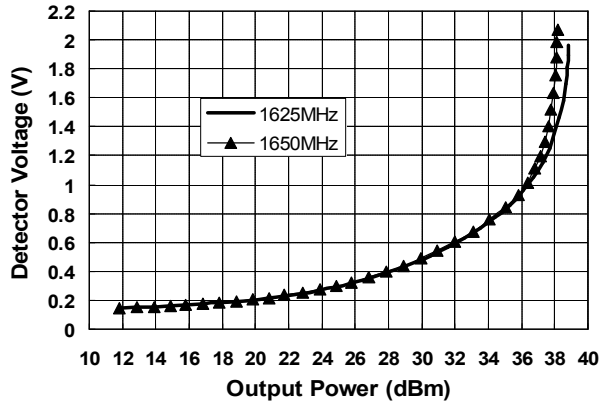


Figure 7. Detector voltage vs output power (CW).

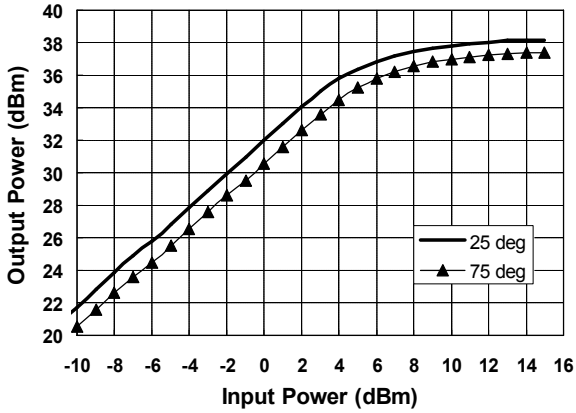


Figure 8. Output power vs input power over temperature at 1650 MHz.

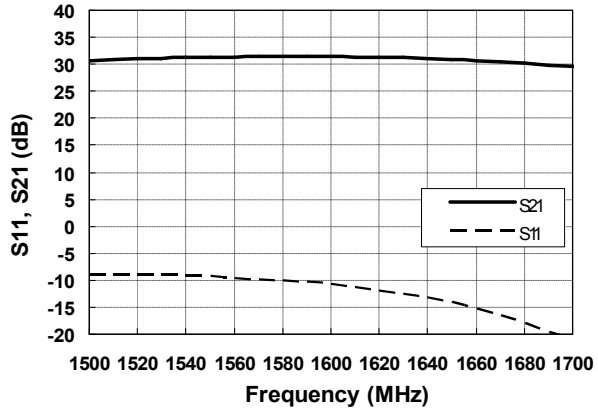


Figure 9. S parameters (S11 and S21) over frequency at room temperature.

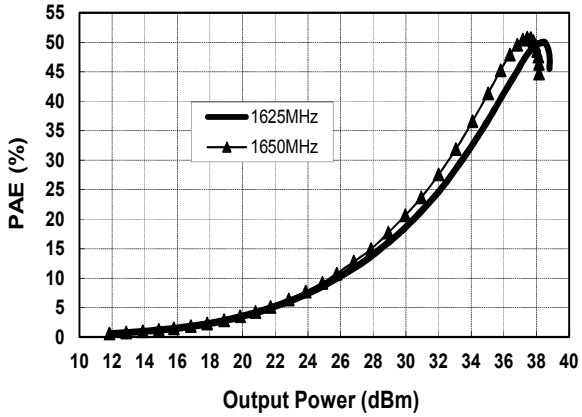


Figure 10. Power Added Efficiency (PAE) vs output power over frequency.

Circuit Design Configurations

The following general design guidelines should be followed in order to obtain optimum performance:

1. Ground connections should be made physically short.
2. The ground pad of LXK6618 has dual purposes – as both electrical grounding and thermal shunt connections. A dense via array should be used under the ground pad to provide thermal conduit for heat dissipation. It is important to understand that the circuit board is used as the heat sink. Therefore, the via connection to ground pad should be designed to allow maximum heat dissipation to the circuit board.
3. Bypass capacitors should be used on the supply voltage circuit trace. Usually a small capacitor (i.e. 100pF) should be placed near the chip, while a larger capacitor (i.e. 0.1uF) is used further away.
4. RF input and output lines should have good isolation from each other to avoid cross talks and coupling. This is important for the device stability. Solid grounds should be place on both sides of RF input and output traces to provide good shielding and isolation.

Application Circuit Notes

VCCB(pin2) Voltage supply for bias circuit. This voltage is typically set to +5 V and requires bypass capacitors.

VCC1(pin3) Voltage supply for the first stage circuit. This voltage is typically set to +5 V and requires bypass capacitors. This pin can be tied to VCCB with sufficient bypassing capacitors.

PDET(pin4) Power detector output voltage. There is an integrated power detector on chip. This pin can be directly sampled to measure the output power. No external resistors or capacitors are required.

RF_IN(pin7) RF input. The device is internally matched to 50 Ohms at the input. In addition, a DC blocking capacitor is included on the chip for RF input.

VREFD(pin9) Power detector reference voltage. This pin supplies voltage for power detector. Typically this pin can be tied to VREF1 and VREF2.

VREF1(pin10), VREF2(pin11) Bias reference voltage for PA. The applied voltage can be from 2.6 V to 3.0 V. These pins can also be used as PA enable pin and may be pulled down to 0 V to disable the PA.

RF_OUT(pin16-20) RF output and voltage supply for the output stage. The bias voltage for the output stage is provided through these pins. An external output matching network is required to obtain optimum load impedance.

Evaluation Board Description

The LXK6618 evaluation board is used to test the performance of the device. Application schematic diagram is provided in Figure 11. An assembly drawing for the evaluation board is shown in Figure 12.

Package Dimensions

The PCB layout footprint for LXK6618 is provided in Figure 12. Typical part marking and the 20-pin QFN package dimension are provided in the package diagram.

Package and Handling Information

Since the device is a moisture sensitive part, it must be baked prior to shipping and placed into the pockets of the carrier tape. Otherwise, problems related to moisture absorption may occur during solder assembly process when the device is subjected to high temperature.

Care must be taken when attaching the device, whether it is done manually or in a production solder reflow environment.

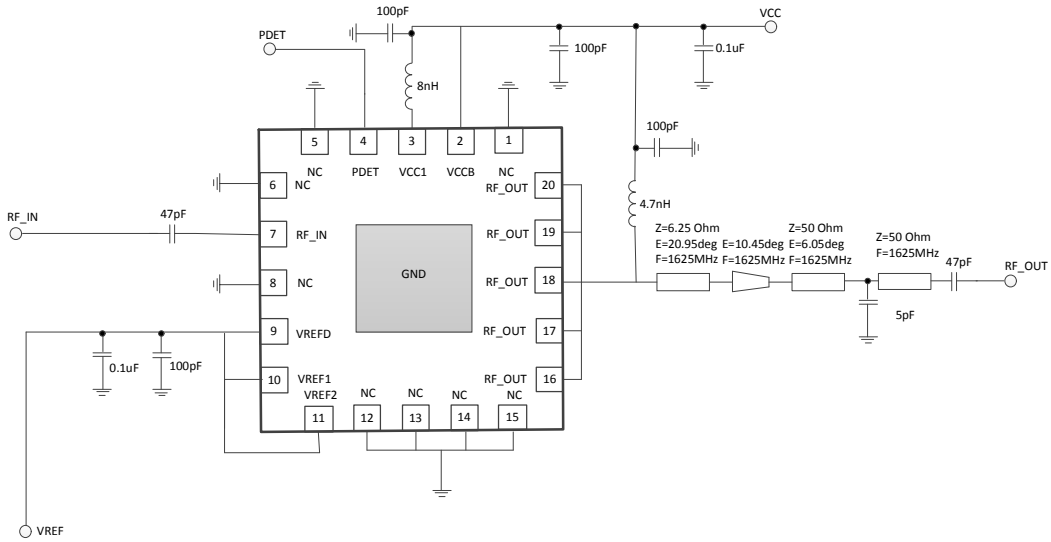


Figure 11. LXK6618 application schematic for 1625MHz operation.

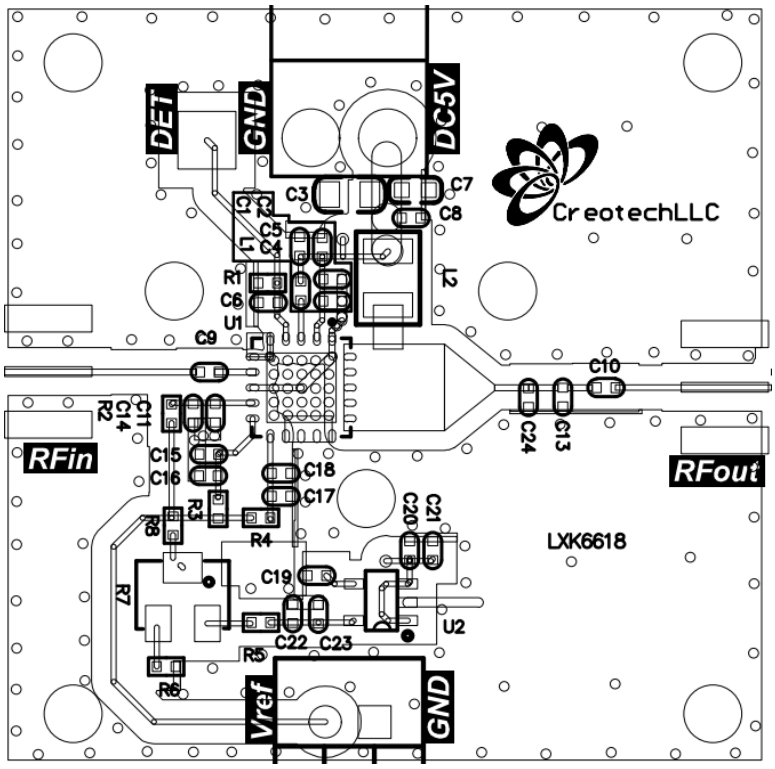
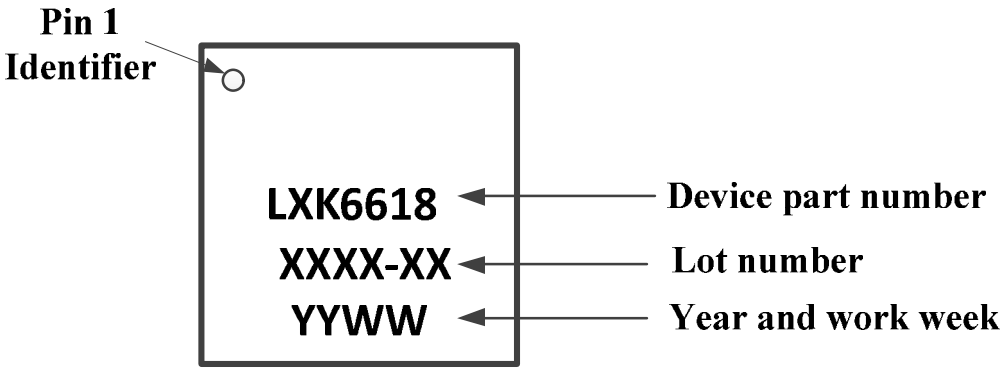
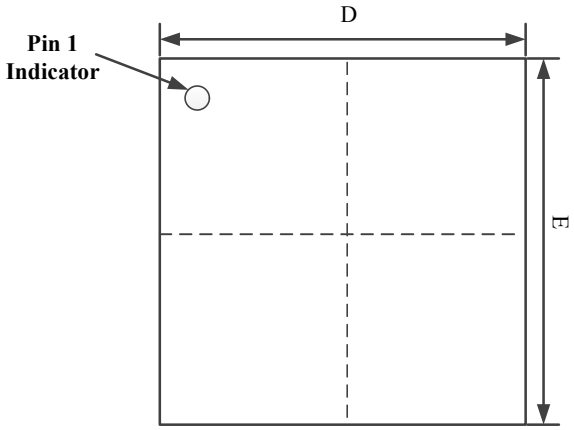


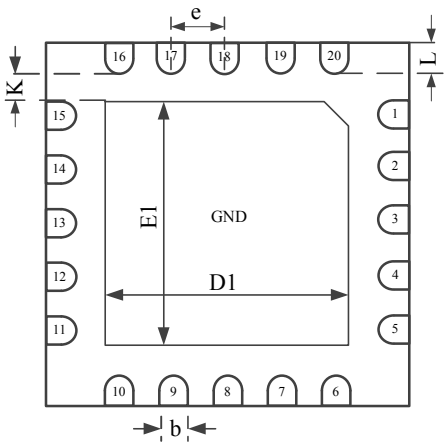
Figure 12. LXK6618 Evaluation Board Assembly Drawing

Package diagram:

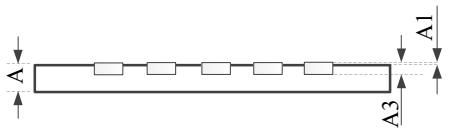




Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.7	0.8	0.028	0.031
A1	0	0.05	0.0	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.400	3.600	0.134	0.142
E1	3.400	3.600	0.134	0.142
K	0.2MIN.		0.008MIN.	
b	0.250	0.350	0.010	0.014
e	0.800TYP		0.031TYP	
L	0.274	0.426	0.011	0.017

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
LXK6618 PA	LXK6618	EVB-LXK6618-01